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Description

SAR ADC Providing Digital Codes with High Accuracy and High Throughput Performance

Background of Invention

[0001] *Field of the Invention*

[0002] The present invention relates to analog to digital converters (ADCs), and more specifically to a successive approximation (SAR) ADC operating with both high accuracy and (high) throughput performance.

[0003] *Related Art*

[0004] Analog to digital converters (ADCs) are used to generate a sequence of digital codes representing the respective signal levels of an analog signal as is well known in the relevant art. In general, an ADC receives a reference voltage also as input, with the voltage indicating the maximum input voltage level.

[0005] Assuming the ADC is to generate an N-bit digital code, a

digital code ideally equals (Vin * 2^N/Vref), wherein Vref, Vin, * and / respectively represent the reference voltage, voltage level of a sample of the input signal, multiplication operator and division operator. In addition, a voltage level corresponding to one least significant bit (LSB) equals (Vref / 2^N).

[0006] ADCs often employ successive approximation principle (SAP) for such a conversion. ADCs implemented using SAP are generally referred to as SAR (successive approximation register) ADCs as a register is used to store the codes used to generate an intermediate analog signal.

[0007] In a typical SAP based implementation, each bit of a digital code (with the digital code representing a sample of the analog signal) is determined in a single iteration, starting from the most significant bit. To determine the most significant bit, the most significant bit is set to a specific logical value (e.g., 1) and the following bits to the other logical value (0), and the resulting number is converted to an intermediate analog signal (generally using a digital to analog converter (DAC), contained in the ADC).

[0008] Assuming the specific logical value equals 1, the value of the most significant bit of the digital code is determined to equal 0 if the sample of the analog signal has less volt-

age than the intermediate analog signal, or else to 1. The next significant bit may be set to 1 (while setting the most significant bit to the determined value) and the following bits to 0, and the resulting number is used to generate a new intermediate analog signal.

[0009] The new intermediate analog signal is compared with the sample of the analog signal to determine the corresponding (next significant) bit of the digital code. The approach is continued until all the bits of the digital code are determined. Other digital codes representing an analog signal may be generated at a desired sampling interval.

[0010] Speed of a SAR ADC is typically determined by the time duration to perform each iteration. The time duration depends on several factors. One of such factors is the time taken by a DAC to generate an intermediate analog signal corresponding to the digital code in each iteration. There is a general need to increase speeds (or throughput performance) of ADCs, and accordingly it may be desirable to reduce the time taken to generate an intermediate analog signal corresponding to a digital code.

[0011] One challenge presented in such reduction is that the load that needs to be driven by a reference voltage, changes as bits are resolved, and the reference voltage changes tran-

siently due to the changing load. At least when SAR ADCs need to operate at a high throughput performance, only a small time window (duration) may be available to resolve additional bits, and the value of the digital code may deviate from the ideal value depending on the difference of the offered reference voltage from the ideal reference voltage while the bits are resolved.

[0012] The degree of change may be different as different bits are being resolved. At least in situations when the change exceeds a threshold voltage equaling the resolution (voltage level equaling one least significant bit value) of the ADC, the output may deviate from an accurate value, and is undesirable.

[0013] The problem may be compounded with respect to high resolution ADCs, since the threshold voltage is inversely proportional to the ADC resolution.

[0014] Another challenge presented in reduction of time to generate an intermediate analog signal, is that the components used in DAC may need certain time to settle to the voltage level of reference voltage. If the time duration is not enough for the components to settle, the signal level of the intermediate analog signal may not represent the digital code accurately in each iteration. Even in such a

situation the output digital code of an ADC may deviate from an ideal (accurate) value.

[0015] One approach to ensuring accurate digital codes is to decrease the throughput performance (speed or number of codes generated per second) of operation of an ADC, such that additional time is available for the various voltage levels to settle. Unfortunately, it is often desired to provide high throughput performance. What is therefore required is a SAR ADC, which provides accurate digital codes at high throughput performance.

Brief Description of Drawings

[0016] The present invention will be described with reference to the following accompanying drawings.

[0017] Figure (Fig.)1 is a block diagram illustrating the details of an example embodiment of a successive approximation analog to digital converter (SAR ADC).

[0018] Figure 2A is a circuit diagram illustrating the details of operation of a digital to analog converter (DAC) in a sampling phase in one prior embodiment.

[0019] Figure 2B is a circuit diagram illustrating the details of a DAC in a conversion phase in one prior embodiment.

[0020] Figure 3 is a block diagram illustrating the details of a SAR ADC according to an aspect of the present invention.

[0021] Figure 4 is a flow chart illustrating the manner in which the accuracy of a digital code may be improved at the output of a high speed SAR ADC according to an aspect of the present invention.

[0022] Figure 5 is a circuit diagram illustrating the details of a DAC according to an aspect of the present invention.

[0023] Figure 6 is a flow chart illustrating the manner in which a ADC may be implemented with high throughput performance and high SNR according to an aspect of the present invention.

[0024] Figure 7 is a block diagram illustrating the details of a SAR ADC providing high SNR and high throughput performance in an embodiment of the present invention.

[0025] Figure 8 is a block diagram illustrating the manner in which the accuracy of digital codes generated by the embodiment of Figure 7 can be improved in an embodiment of the present invention.

[0026] Figure 9 is a block diagram illustrating an example system in which the present invention can be implemented.

[0027] In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding

reference number.

DETAILED DESCRIPTION

[0028] *1. Overview*

[0029] An aspect of the present invention provides SAR ADCs which can operate at a high speed (throughput performance) while providing digital codes of high accuracy as well. A first reference voltage is used to generate an equivalent voltage corresponding to previous generated bits and a second reference voltage is used to generate equivalent voltage corresponding to the bits being presently resolved.

[0030] Since the first reference voltage is used to generate equivalent voltage corresponding to the resolved bits (which do not change in the same conversion phase), the first reference voltage may not change due to the load offered by a DAC used in the conversion iterations. Accurate digital codes may be generated as a result.

[0031] In addition, as the second reference voltage is used to resolve only a portion of the bits (i.e., small number of bits) at any time, the load may not affect the voltage level much. As a result, a next bit can be resolved quickly (without having to allow for substantial settling time),

thereby enhancing the throughput performance of ADCs. Thus, ADCs may be implemented with high speed as well as with high accuracy.

[0032] Another aspect of the present invention improves signal to noise ratio (SNR) of a high speed SAR ADC by using a high speed DAC in combination with a DAC providing high SNR. SNR generally refers to the ability of an ADC to generate a digital code accurately independent of any noise that may otherwise affect the accuracy. In an embodiment, the high speed DAC resolves the most significant bits (MSBs) in the digital code accurately at a high speed (compared to the DAC with high SNR). The resolved MSBs are used to set the corresponding MSBs of the digital code in the high SNR DAC. The remaining bits of the digital code are generated using the DAC providing high SNR.

[0033] By using high speed DACs (which generally operate faster), the overall throughput performance of a SAR ADC is enhanced. By using a high SNR DAC to resolve the LSBs, the SNR of the ADC may also be enhanced. Thus, high speed ADCs providing high SNR as well as accurate digital code may be provided according to several aspects of the present invention.

[0034] Various aspects of the present invention are described be-

low with reference to an example problem. Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well_known structures or operations are not shown in detail to avoid obscuring the invention.

[0035] *2. Example Environment*

[0036] Figure 1 is a block diagram illustrating the details of an example prior embodiment of ADC 100, which can be improved according to several aspects of the present invention. SAR ADC 100 is shown containing comparator 110, SAR logic 120, digital to analog converter (DAC) 130, and buffer 190. Each component is described in detail below.

[0037] Comparator 110 compares an intermediate analog signal received on path 131 with a voltage level Vmid (equaling Vdd/2 in an example embodiment, wherein Vdd represents a supply voltage) on path 102, and provides the result of the comparison (iteration status) on path 112. In an embodiment, the result equals a logical value '1' if a

sample of an analog signal on path 101 is greater than the signal value corresponding to the intermediate digital value (described below), else the result equals a logical value of '0'. Comparator 110 can be implemented in known way.

[0038] SAR logic 120 determines the digital code corresponding to a sample (provided on path 101) using successive approximation principle by interfacing with comparator 110 and DAC 130. In general, SAR logic 120 sends an intermediate digital value during each iteration to determine a bit, and generates the digital code based on the determined bits. The digital code is provided on path 199. Clock 122 controls the duration of each iteration. In an embodiment, clock 122 operates with different durations in different iterations as described in further detail in sections below.

[0039] DAC 130 samples the analog signal received on path 101 before the first iteration during conversion. DAC 130 then generates intermediate analog signal 131 having a voltage level equaling (Vmid _ Vinp + a voltage level corresponding to an intermediate digital value received on path 123) in each iteration (in which a bit of the digital code is determined), wherein Vinp represents the voltage level of the

sampled analog signal.

[0040] The voltage level corresponding to intermediate digital value is generated using a reference voltage received on path 193. For example, assuming that the intermediate digital value (on path 123) equals Q and reference voltage 193 equals Vref, then the voltage level corresponding to the digital value equals $(Vref * Q)/2^N$, wherein N represents the number of bits in the digital code generated by the ADC.

[0041] Buffer 190 generates reference voltage 193 from an external voltage received on path 191. In general, reference voltage 193 needs to be at a constant predetermined level during all the iterations for the digital code to be generated accurately. The reference voltage may not be at such a level for reasons noted above in the background section. As a result, the digital code may not be generated accurately.

[0042] An aspect of the present invention enables the digital code to be determined accurately at a high speed. Such a feature is achieved by implementing DAC 130 consistent with the principles underlying various aspects of the present invention. The principles may become clearer by understanding operation of the DAC in example prior em-

bodiments. Accordingly, the operation of prior DAC is described first with reference to Figures 2A and 2B.

[0043] *3. Prior DAC*

[0044] Figures 2A and 2B are circuit diagrams illustrating the details of DAC 130 (illustrated with reference to paths 101, 193, 123 and 131) in sampling phase and conversion phase respectively in one prior embodiment. As is well known, the input signal (on path 101) is sampled in the sampling phase, and the sample is converted into a digital code in multiple iterations (with one bit determined in each iteration) of the conversion phase.

[0045] Continuing with reference to Figure 2A, DAC 130 is shown containing capacitors 210_1 through 210_N and 230_1 through 230_6, and switches 220_1 through 220_N and 260. One end of all the capacitors (top plate) is coupled to Vmid on path 102. The other end (bottom plate) of capacitors 210_1 through 210_N is connected to a sample of analog signal on path 101 by a corresponding switch. The other end of capacitors 230_1 and 230_3 is connected to Vref 193, and of capacitors 230_2 and 230_4 is connected to ground. The operation of capacitors 210_1 through 210_N and 230_1 through 230_4 in sampling phase is described below and the operation of capacitors 210_1

through 210_N and 230_1 through 230_6 is described in conversion phase with reference to Figure 2B.

[0046] Switches 220_1 through 220_N and 260 are closed in the sampling phase, causing the analog signal on path 101 to be sampled on capacitors 210_1 through 210_N. Each capacitor 210_1 through 210_N charges through sample 101 and Vmid 102. Each of capacitors 230_1 and 230_3 charges through Vref 193 and Vmid 102, and each of capacitors 230_2 and 230_4 charges through Vmid 102 and ground. The voltage corresponding to total charge due to all capacitors is provided on path 131. Capacitors 210_1 through 210_N, 230_5 and 230_6 together resolve N_bit digital code in conversion phase and capacitors 230_1 through 230_4 together correct error in the resolved bits of N_bit digital code, as described below in further detail with reference to Figure 2B.

[0047] Figure 2B is a circuit diagram illustrating the details of the DAC (of Figure 2A) in the conversion phase. In an embodiment, high speed SAR ADC may be implemented by resolving some bits of the N-bit digital code at a high speed and remaining bits at a low speed by using a combination of high speed and low speed clock pulses contained in clock signal 122.

[0048] Assuming that the N-bit digital code is divided into (P+Q+R)bits, then the first P-MSBs of N-bit digital code are resolved at a high speed by providing a high speed clock signal on path 122 since MSBs may not be required to be accurate and can be resolved at high speed. The next Q-MSBs of the N-bit digital code are resolved at a speed less than that of the first P- MSBs. The remaining R-bits are resolved at a low speed by receiving a low speed clock signal on path 122.

[0049] Briefly, during conversion phase, capacitors 210-1 through 210-P are operational while resolving the P-bits, capacitors 210-P+1 through 210-P+Q are operational while resolving the Q-bits, and capacitors 210-P+Q+1 through 210-N are operational while resolving the remaining R-bits in the N-bit digital code. Capacitors 230-1 through 230-4 corrects the error in the resolved bits.

[0050] Capacitors 230-5 and 230-6 facilitate the selection of capacitance values of capacitors 210-1 through 210-N to be practically feasible values if N is a large number as described in further detail below.

[0051] In an embodiment, the effective capacitances of capacitors at positions 210_1 through 210_N need to respectively equal C, C/2, C/4, etc. to generate the intermediate ana-

log signal in increments of binary weight (of voltage) in each iteration as required for a SAR operation. In such an embodiment, the lowest capacitance required is $C/2^N$. In practice, realizing such capacitors with such a low capacitance may provide substantial challenges if N is a large number. Series capacitors 230-5 through 230-6 are used to avoid the requirement of such low capacitance value as described below.

[0052] Capacitor 230-5 is connected in series between the P-set of capacitors (210-1 through 210-P) and Q-set of capacitors (210-P+1 through 210-P+Q). The capacitance value of capacitor 230-5 is chosen such that the effective capacitance of capacitor 230-5 and the first capacitor 210-P+1 in the Q-set of capacitors equals half that of 210-P, as desired. In an embodiment, the capacitance value of capacitor 210-P+1 equals C and the remaining capacitance values of capacitors in the Q-set of capacitors equal C/2, C/4....$C/2^Q$ to provide effective binary weighted voltage. As a result, capacitors with low capacitance may not be required since Q is less than N.

[0053] The description is continued below with reference to the manner in which capacitors 210-1 through 210-N and 230-1 through 230-6 operate to generate an intermedi-

ate voltage in binary weighted format.

[0054] During the conversion phase, switch 260 is opened to force the total charge on top plates of all capacitors to remain the same (equal to) as in the sampling phase. The bottom plates of capacitors 210-1 through 210-N are either connected to Vref on path 193 or ground on path 221 by respective switches 220_1 through 220_N based on the corresponding bits of intermediate digital value 123.

[0055] While resolving the first P-MSBs, intermediate digital value 123 represents the digital value corresponding to the P-bits, and switches 220-1 through 220-P are controlled by the P-bits in the intermediate digital value to connect capacitors 210-1 through 210-P to either Vref or ground. For example, assuming P equals 6 (intermediate digital value corresponding to the P-bits starting from MSB equals '101000'), switches 220-1 and 220-3 are connected to Vref 193 and the remaining switches are connected to ground.

[0056] If the voltage on bottom plates of the capacitors is changed, the voltage on top plates would also change in a similar manner to maintain the same charge. Due to the operation of switches 220_1 through 220_P, the voltage

on bottom plates of the capacitors is controlled by the intermediate digital value on path 123. Therefore, a change in intermediate digital value causes a similar change in the voltage at top plates (Vtop) on path 131. As a result, DAC provides the intermediate analog signal on path 131 with a voltage level in the form of binary weighted increments due to the selection of binary weighted capacitances for the capacitors in the above example embodiment.

[0057] SAR logic 120 uses the comparison result of the voltage on path 131 with a voltage on path 102, and determines the corresponding bit in the N-bit digital code in each iteration. As may be noted that, intermediate voltage (voltage level of intermediate analog signal 131) on path 131 may not equal exactly to the voltage on path 102 even after resolving the P-bits, and the difference may be viewed as an error. The P-bit digital code may need to be corrected if the error is more than the resolution of the ADC. The manner in which such correction may be performed is described below with reference to capacitors 230-1 and 230-2.

[0058] Once the first P-bits are resolved, capacitors 230-1 and 230-2 correct the error in the P-bit digital code in negative and positive directions respectively. As capacitors

230-1 and 230-2 are connected to respective voltages Vref 193 and ground 221 during both sampling and conversion phases, the voltage corresponding to the capacitors may not affect the resolved bits. If the comparison result indicates that the intermediate voltage is greater than voltage 102, then the error will be corrected in negative direction by connecting capacitor 230-1 to ground. As a result, the intermediate voltage level may be reduced.

[0059] Similarly, if the comparison result indicates the intermediate voltage is less than voltage 102, then the error will be corrected in positive direction by connecting capacitor 230-2 to Vref 193. As a result, the intermediate voltage will be increased to correct the error in the positive direction.

[0060] After resolving the P-bits and correcting the error, the residue voltage is used to resolve the next Q-bits and next the remaining R-bits in a similar manner. Capacitors 230-3 and 230-4 are used similar to capacitors 230-1 and 230-2 respectively to correct the error in the Q-bits. In an embodiment, the capacitance of each of capacitors 230-1 and 230-2 is selected equaling the capacitance of capacitor 210-P, and the capacitance of each of capacitors 230-3 and 230-4 is selected equaling the capacitance of

capacitor 210-P+Q. The problems with such a prior DAC are described below.

[0061] *4. Problems with the Prior DAC*

[0062] One problem with the prior DAC described with respect to Figures 2A and 2B is the capacitance load offered on buffer 190 by switching the connections of capacitors 210-1 through 210-N changes based on intermediate digital value on path 123. After resolving the P-bits, the capacitance load increases while resolving the next Q-bits since the capacitance value of capacitor 210-P+1 is chosen to be a large value ('C'), which causes a correspondingly high change in the voltage level of Vref 193. Vref 193 needs to be at least N-bit accurate (i.e., the change in Vref 193 can be with in the range of $Vref/2^N$) to generate an accurate N-bit digital code. Thus, Vref 193 needs to be (P+Q) bits accurate while resolving the Q-bits and N-bits accurate while resolving the remaining R-bits in the N-bit digital code.

[0063] However, switching the large capacitance ('C') to Vref 193 according to intermediate digital value, may cause a large change in Vref 193, which causes an error in the intermediate voltage on path 131. As a result, the N-bit digital code at the output may not be accurate.

[0064] In addition, the accuracy may be adversely impacted due to the settling requirement of large capacitors in DAC. As the capacitance of capacitors (for example, of 210-1, 210-(P+1), etc.) is large, then such capacitors will require long time to settle to the voltage level of Vref 193 in the desired time duration (less than one clock cycle of clock 122). As a result, the intermediate voltage on path 131 may not be accurate, which may cause inaccuracy in the digital code at the output of a SAR ADC. Several aspects of the present invention increase the accuracy of the output digital code while resolving the bits at a high speed as described below in further detail with reference to Figure 3.

[0065] *5. SAR ADC*

[0066] Figure 3 is a block diagram illustrating the details of SAR ADC 300 according to an aspect of the present invention. SAR ADC 300 is shown containing comparator 310, SAR logic 320, digital to analog converter (DAC) 330, and buffers 390 and 350. In the embodiment(s) of Figure 3, buffers 390 and 350 are shown contained in SAR ADC 300. However, in alternative embodiments, buffers 390 and 350 are provided external to SAR ADC 300. Each component is described in detail below.

[0067] Paths 301, 302, 312, 322, 323, 331 and 393 operate sim-

ilar to paths 101, 102, 112, 122, 123, 131 and 193 of Figure 1 respectively. Briefly, path 301 receives an analog signal to be sampled and converted into an N-bit digital code. Path 302 receives Vmid voltage as described above with reference to Figure 1. Path 312 contains a comparison result of intermediate analog signal on path 331 and Vmid 302. Path 323 contains intermediate digital value 323 generated in each iteration of conversion phase. Path 393 contains a reference voltage and path 353 contains another reference voltage.

[0068] Comparator 310, SAR logic 320 and buffer 390 respectively operate similar to comparator 110, SAR logic 120 and buffer 190 of Figure 1. The remaining components of Figure 3 are described below.

[0069] Each of buffers 350 and 390 generates reference voltage Vref on paths 353 and 393 respectively. The reference voltages thus generated are used to generate N-bit digital codes accurately and with high throughput rate (speed) as described below.

[0070] DAC 330 generates an intermediate analog signal (on path 331) corresponding to intermediate digital value 323 using both reference voltages 353 and 393. As the load caused by DAC 330 is distributed across multiple refer-

ence voltages, each reference voltage may be less susceptible to changes due to the load imposed by operation of DAC 330. In an embodiment described below, one reference voltage is used to operate the portions corresponding to the resolved bits, and another reference voltage is used to operate the portions corresponding to the bits presently being resolved. Digital codes may be generated accurately as a result.

[0071] The implementation of DAC may need to be implemented taking into account various other design considerations as well. In an example implementation described below, the accuracy of digital code depends on the two reference voltages 353 and 393 being substantially equal. For example, the difference of the two voltages may need to be (N-P) bit accurate to generate an accurate N-bit digital code.

[0072] Implementing buffers, which generate such substantially equal voltages may be challenging for reasons such as variation in the inherent characteristics of the components used in buffers 390 and 350, etc. An aspect of the present invention enables DAC 330 to generate accurate N-bit digital codes, while operating with reference voltages which potentially deviate by more than (N-P) bit LSB

equivalent voltage, as described below.

[0073] *6. Method*

[0074] Figure 4 is a flowchart illustrating the manner in which multiple reference voltages may be used to resolve N-bit digital code corresponding to a sample of an analog signal according to an aspect of the present invention. The method is described with reference to Figure 3. The method begins in step 401, in which control immediately passes to step 410.

[0075] In step 410, DAC 330 receives an analog sample, from which an N_bit digital code is sought to be generated. DAC 330 may sample and store the voltage level of the analog sample.

[0076] In step 420, DAC 330 generates P MSBs (P-bit digital code) of the N-bit digital code from the analog sample using one of the two reference voltages (e.g., first reference voltage), wherein P is less than N, and P and N are integers. To generate an accurate N-bit digital code, the first reference voltage needs to be at least P-bit accurate (that is, the first reference voltage should not deviate by more than $1/2^P$ fraction of the desired Vref voltage).

[0077] In step 440, DAC 330 then generates the next Q bits (Q_bit digital code) of the N-bit digital code while using

the first reference voltage to generate the equivalent voltage (which considers the weight of the bit positions as well as bit values) corresponding to the P bits, and using a second reference voltage to resolve the next Q bits, wherein (P+Q)<N. The second reference voltage needs to be at least Q-bit accurate to generate an accurate N-bit digital code.

[0078] In step 460, DAC 330 generates the next R bits (R_bit digital code) while using the first reference voltage to generate the equivalent voltage corresponding to both P and Q bits, and using a second reference voltage to resolve the next R bits. Step 460 is repeated until all the bits in N-bit digital code are resolved. The method ends in step 499.

[0079] Thus, one of the buffers is used to provide the reference voltage to (portions of the circuit corresponding to) the previously resolved bits and another buffer is used to provide another reference voltage to the bits presently being resolved. The manner in which such an approach may generate accurate digital codes even if the two reference voltages are not substantially equal, is described below with reference to details of DAC 330 in one embodiment.

[0080] *7. DAC*

[0081] Figure 5 is a circuit diagram illustrating the details of DAC

330 in an embodiment of the present invention. For conciseness, DAC 330 is described in comparison to Figures 2A and 2B. DAC 330 is shown containing capacitors 510-1 through 510-N and 530-1 through 530-6, and switches 520-1 through 520-N and 560. The operation of each component is described in further detail below.

[0082] Capacitors 510-1 through 510-N, and 530-1 through 530-6, and switches 520-1 through 520-N and 560 may be operated similar to capacitors 210-1 through 210-N, and 230-1 through 230-6, and switches 220-1 through 220-N and 260 respectively as in Figures 2A and 2B to determine a N-bit digital code. However, in comparison to switches 220-1 through 220-N (which contain only three connection points), each of switches 520-1 through 520-N contains one more connection point. The additional connection point enables a second reference voltage to be received (to connect to corresponding capacitor) according to several aspects of the present invention, as described below.

[0083] As described above, DAC 330 receives an analog sample on path 301 in a sampling phase, in which switches 520-1 through 520-N are connected to path 301. DAC 330 converts the analog sample into an N-bit digital code in the

conversion phase. For illustration, the N-bit digital code is assumed to be divided into (P+Q+R) bits, each of which is potentially generated at different speeds to provide the final N-bit digital code at a high speed. The speed of resolving each of P, Q and R bits is controlled by a clock signal received on path 322 of Figure 3. The manner in which reference voltages on paths 393 and 353 are connected to resolve the bits is described below.

[0084] Reference voltage 393 is used to resolve the first P-bits (MSBs of N-bit digital code). Switches 520-1 through 520-P are controlled by the P-bits in the intermediate digital value received on path 323 to connect each of capacitors 510-1 through 510-P to either Vref 393 or ground (depending on whether the corresponding bit is 0 or 1). All the remaining capacitors 510-P+1 through 510-N are connected to ground or Vref 393 according to the corresponding bits in intermediate digital value 323 by the corresponding switches 520-P+1 through 520-N. The P-bits may be resolved in P-iterations by the appropriate operation of comparator 310 and SAR logic 320. Capacitors 530-1 and 530-2 operate to correct the error in the resolved P-bits in the (P+1) iteration similar to capacitors 230-1 and 230-2.

[0085] Continuing with resolving the N-bits, once all the P-bits are resolved, the next Q-bits are resolved by using both reference voltages 393 and 353. Reference voltage 393 is used to provide the required reference voltage to capacitors 510-1 through 510-P. Each capacitor 510-1 through 510-P is connected to either Vref 393 or ground according to the corresponding resolved bit value.

[0086] That is, when the P MSBs are resolved first, switches 520-1 through 520-P are used to connect corresponding capacitors 510-1 through 510-P to Vref 393 (or ground, depending on the corresponding bit in the intermediate digital value). On the other hand, when the remaining (N-P) are resolves, switches 520-1 through 520-P are used to connect corresponding capacitors 510-1 through 510-P to Vref 353 (or ground). The remaining capacitors 510-P+1 through 510-N may also be operated similarly (i.e., connected to Vref 393 while corresponding bits are being resolved and then to Vref 353 after resolution).

[0087] Reference voltage 353 provides the reference voltage to capacitors 510-P+1 through 510-P+Q (while the Q bits are being resolved). Each capacitor 510-P+1 through 510-P+Q is connected to either Vref 353 or ground by operating corresponding one of switches 520-P+1

through 520-P+Q based on the corresponding one of the bits of the intermediate digital value 323. The Q-bits are thus resolved in Q-iterations by the appropriate operation of comparator 310 and SAR logic 320.

[0088] Capacitors 530-3 and 530-4 operate to correct the error in the resolved (P+Q)- bits in Q+1 iteration similar to capacitors 230-3 and 230-4. Even though, capacitor 530-4 is shown connected to Vref 353, each of capacitors 530-3 and 530-4 is either connected to Vref 393 or ground after Q+1 iteration based on the result of error correction.

[0089] Similarly, the remaining R-bits are also resolved by using the two reference voltages 393 and 353. In particular, the required reference voltage to capacitors 510-1 through 510-P+Q is provided using Vref 393 and to capacitors 510-P+Q+1 through 510-N using reference voltage 353.

[0090] It may be noted that reference voltage 393 needs to be of P-bit accuracy (deviation by less than $1/2^P$ of the desired reference voltage) while resolving the P-bits. If P is small, for example 6, then 6-bit accuracy can easily be achieved. Similarly, reference voltage 353 needs to be only Q-bit accurate while resolving Q-bits. Even though, reference voltage 353 needs to be only Q-bit accurate, intermediate voltage on path 331 is provided with (P+Q) bit accuracy

while resolving Q-bits since any variation in reference voltage 353 is divided by the capacitance of series capacitor 530-5. As a result, the accuracy and the difference between reference voltage generated by buffers 390 and 350 may also be reduced (which may otherwise require (N-P) bit accuracy in prior DAC of Figure 2B). When the accuracy requirements are reduced, low power buffers may be advantageously used to generate the reference voltages.

[0091] In addition, the approach of above may generate accurate N-bit digital codes even if the two reference voltages are not substantially equal. Such an accuracy is achieved since a single reference voltage is used to generate the intermediate analog signal (from the intermediate digital value) corresponding to the resolved bits. In addition, the error correction techniques (such as that described above) correct any deviations that may have been caused due to a different voltage level being present on the other reference voltage.

[0092] In addition, the load on buffer 390 due to capacitors in DAC 330 may not affect the reference voltage on path 393 since Vref 393 is connected to the capacitors corresponding to the resolved bits, which do not switch their connec-

tions. As a result of constant load on buffer 390, reference voltage 393 may not change much.

[0093] Similarly, the capacitance load on buffer 350 due to the capacitors corresponding to the bits presently being resolved is small, since buffer 350 is used to resolve only a few bits of the N-bit digital code. However, a change in capacitance load may (at least transiently) decrease the voltage level of Vref 353 and cause inaccuracy in the N-bit digital code. Such inaccuracy may be corrected using error correction as described above.

[0094] Therefore, an accurate N-bit digital code may be generated corresponding to a sample of an analog signal by using one reference voltage to provide the voltage to the capacitors corresponding to the resolved bits and another reference voltage to provide the required voltage to the capacitors corresponding to the bits presently being resolved in the N-bit digital code.

[0095] In the design of high speed SAR ADCs, it may be required to provide a high signal to noise ratio (SNR) as well as high throughput performance. As noted above, SNR generally refers to the ability of an ADC to generate a digital code accurately independent of any noise that may otherwise affect the accuracy. It may be appreciated that SNR of

SAR ADCs can be increased by using capacitors with a large capacitance value. However, an increase in capacitance value of capacitors used in a DAC of a SAR ADC may lead to reduction in throughput performance since large capacitors may need more time to settle to the correct value. The manner in which SNR may be increased while providing a digital code at a high speed according to an aspect of the present invention is described below with examples.

[0096] *8. Method of Increasing SNR of a Digital Code While Maintaining High Speed*

[0097] Figure 6 is a flowchart illustrating a manner in which signal to noise ratio (SNR) (and accuracy) of a SAR ADC may be increased while maintaining high speed (throughput performance) in an embodiment of the present invention. The method is described with reference to Figures 3 and 5 for illustration. The method begins in step 601, in which control immediately passes to step 610.

[0098] In step 610, an analog sample is received, from which an N-bit digital code (N being an integer) is to be generated. Each of a high SNR DAC and a high speed DAC (described in steps below) samples and stores the voltage level of the analog sample.

[0099] In step 620, M MSBs of the N_bit digital code are resolved using a DAC operating at a high speed, wherein M is an integer less than N. In an embodiment, high speed DAC is implemented using small (absolute) capacitance values for the capacitors in the DACs, while maintaining the same capacitance values consistent with the design requirements of SAR principles. Small value capacitors generally settle to the final/correct voltage quickly and thus the speed may be increased. The short settling times facilitate accurate determination of the M-bits in a short duration.

[0100] In step 640, M_MSBs of N_bit digital code are set to the M_bits resolved in step 620. In step 660, remaining bits (N_M) of N_bit digital code are resolved using a DAC providing a high SNR, but starting with the M-MSBs set in step 640 as the intermediate digital value. As noted above, high SNR may be achieved by using large capacitance capacitors in a DAC (but with relative ratios being consistent with a SAR implementation). Due to the use of the high SNR DAC, the N-bit digital code may be generated with a high SNR. The method ends in step 699.

[0101] Thus, by using a high speed DAC to resolve the MSBs, the throughput performance is enhanced, and by using a high SNR DAC to resolve the remaining bits, high SNR is at-

tained. The description is continued with reference to an example embodiment implementing at least some of the features described above.

[0102] *9. High SNR SAR ADC Providing Accurate Digital Code at a High Speed*

[0103] Figure 7 is a block diagram illustrating the details of a SAR ADC providing high SNR and generating digital codes at a high speed in an embodiment of the present invention. SAR ADC 700 is described with reference to Figure 3 for illustration. SAR ADC 700 is shown containing high speed DAC 710, high SNR DAC 720, comparators 730 and 740, multiplexer 750, SAR logic 760, and buffers 770 and 780. Each component is described below in detail.

[0104] Buffers 770 and 780 generate reference voltages 771 and 782 from an external voltage received on path 701. Buffers 770 and 780 can be implemented in a known way.

[0105] High speed DAC 710 samples the analog signal received on path 301 in a sampling phase before the first iteration during conversion. DAC 710 generates an intermediate voltage (similar to the voltage level of path 131 of Figure 1) on path 713 from the intermediate digital value received on path 761. Intermediate voltage 713 is generated using a reference voltage received on path 771. DAC 710

may be implemented similar to DAC 130 (or only a portion corresponding to the M-bits), but using low capacitance value capacitors (compared to in DAC 720). DAC 710 generates intermediate voltage 713 accurately since capacitors with low capacitance value settle to reference voltage 771 quickly in the desired time duration (a clock cycle at high speed).

[0106] High SNR DAC 720 also samples the analog signal received on path 301 in a sampling phase before the first iteration during conversion. DAC 720 generates an intermediate voltage on path 724 from the N-bit intermediate digital value received on path 762 and a reference voltage received on path 782 when the (N-M) least significant bits (LSBs) are being resolved. In an embodiment, DAC 720 is also implemented similar to DAC 130, but using high capacitance value capacitors (compared to in DAC 710). such an embodiment, DAC 720 may be provided the N-bit digital values (from SAR logic 760) even when the M MSBs are resolved, which provides the capacitors additional time to settle to the respective final voltages.

[0107] Comparator 730 compares an intermediate analog signal received on path 713 with a voltage level (Vmid equaling Vdd/2 in an example embodiment) on path 302, and pro-

vides the result of the comparison (iteration status) on path 735. Comparator 740 operates similarly except that input signal on path 724 is compared with Vmid 302, and output is generated on path 745.

[0108] Multiplexer (mux) 750 selects one of the results received on paths 735 and 745 under the control of SAR logic 760. The comparison result on path 735 is selected while determining the first M-bits, and comparison result on path 745 is selected while determining the remaining (N-M) bits. Mux 750 provides the selected comparison result on path 756.

[0109] SAR logic 760 determines the N-bit digital code corresponding to a sample (provided on path 301) using successive approximation principle by interfacing with mux 750, and DACs 710 and 720. In general, SAR logic 760 sends an intermediate digital value during each iteration to determine a bit. Clock 322 controls the duration of each iteration.

[0110] As described above, only a M-bit value may need to be sent on path 761 while resolving the first M-bits. A N-bit value may be sent on path 762 at least while resolving the remaining (N-M) bits. SAR logic 760 may control the operation of mux 750 to cause the input value on path 735

to be selected while resolving first M-bits and the input value on path 745 to be selected while resolving the remaining bits of N-bit digital code.

[0111] It may be noted from the above that high SNR is obtained due to the use of high SNR DAC and high throughput performance is obtained due to the use of high speed DAC. As a result, high speed SAR ADC providing high SNR may be implemented according to several aspects of the present invention.

[0112] One problem with (an embodiment of) high SNR DAC of 720 is that large capacitance may reduce the voltage level of reference voltage 782 and causes an inaccuracy in the N-bit digital code. The accuracy may be increased using techniques described above with reference to Figure 3. Alternative embodiments implemented accordingly are described below with reference to Figure 8.

[0113] *10. Alternative Embodiment*

[0114] Figure 8 is a block diagram illustrating the details of a SAR ADC further improving accuracy of a digital code in an alternative embodiment of the present invention. SAR ADC 800 is described with reference to Figures 3 and 7 for illustration. SAR ADC 800 is shown containing high speed DAC 710, high SNR DAC 820, comparators 730 and 740,

multiplexer 750, SAR logic 760, and buffers 770, 780 and 890. Merely for conciseness, the components introduced in Figure 7 are not described again. All the remaining components are described below in detail.

[0115] High SNR DAC 820 operates similar to DAC 330 of Figure 3, but with buffers 780 and 890 providing the two reference signals. Due to the use of two reference voltages on paths 882 and 892 similar to reference voltages 393 and 353 respectively, the inaccuracy due to error in intermediate voltage 724 may be reduced. In addition, due to the use of high speed DAC to resolve the MSBs, the inaccuracy due to settling of the capacitors corresponding to MSBs in DAC 20 may be reduced. Therefore, SAR ADC 800 provides an accurate digital code at a high speed.

[0116] The approaches described above can be implemented in various systems. The description is continued with reference to an example system in which several aspects of the present invention can be implemented.

[0117] *11. Example System*

[0118] Figure 9 is a block diagram of receiver system 900 illustrating an example system in which the present invention may be implemented. For illustration, it is assumed that receiver system 900 corresponds to a Global Positioning

System (GPS) receiver. However, several aspects of the present invention can be implemented in other communication systems (e.g., mobile phone, etc.). Receiver system 900 is shown containing antenna 901, analog processor 920, ADC 950, and processing unit 990. Each component is described in further detail below.

[0119] Antenna 901 may receive various signals transmitted from satellites, etc. The received signals may be provided to analog processor 920 on path 912 for further processing. Analog processor 920 may perform tasks such as amplification (or attenuation as desired), filtering, frequency conversion, etc., on received signals and provides the resulting signal on path 925. The processed signal may be provided to ADC 950 on path 925.

[0120] ADC 950 converts the analog signal received on path 925 to a corresponding digital value based on SAP. The digital value may be provided to processing unit 990 on path 959 for further processing. ADC 950 may be implemented in a similar manner to ADC 300 of Figure 3 or ADC 700 of Figure 7. In alternative embodiment, ADC 950 may be implemented in a similar manner to ADC 800 of Figure 8. Processing unit 990 receives the recovered data to provide various user applications (such as telephone calls, data

applications).

[0121] Thus, several aspects of the present invention described above can be used to provide a high speed successive approximation type analog to digital converters with accurate digital code while increasing SNR.

[0122] In addition, various modifications can be made to the embodiments/approaches described above without departing from the scope and spirit of several aspects of the present invention. For example, the DACs are shown implemented using capacitors, however, the DACs can be implemented in several other ways as is well known in relevant arts.

[0123] Similarly, even though the description of above is provided with reference to single-ended circuits, the approaches described above can be extended to differential circuits, as will be apparent to one skilled in the relevant arts by reading the disclosure provided herein.

[0124] *12. Conclusion*

[0125] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above described exemplary embodiments, but should be defined

only in accordance with the following claims and their equivalents.